

Project Name :A14IEXX Rev:A0

Platform : PineView -D + TigerPoint + DDR3

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M/B Schematic Version Change List

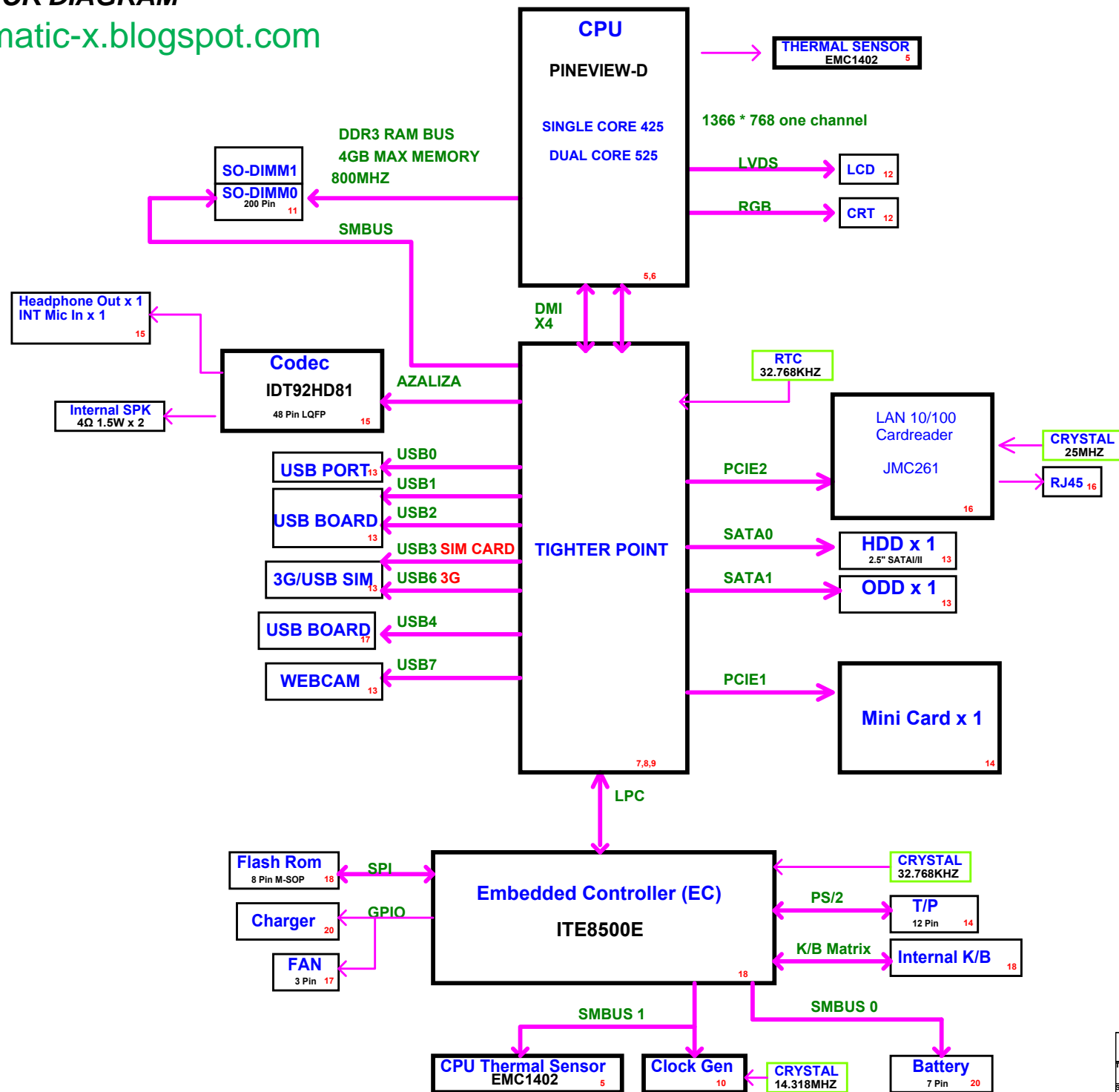
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note
					Main
					Main
					2ND

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM

www.schematic-x.blogspot.com



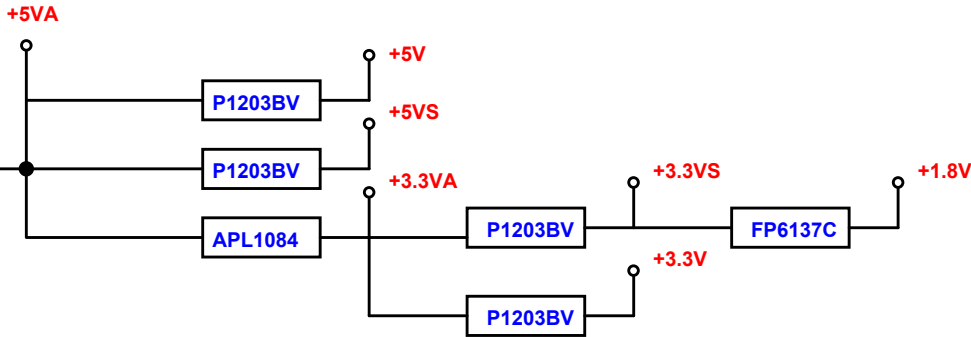
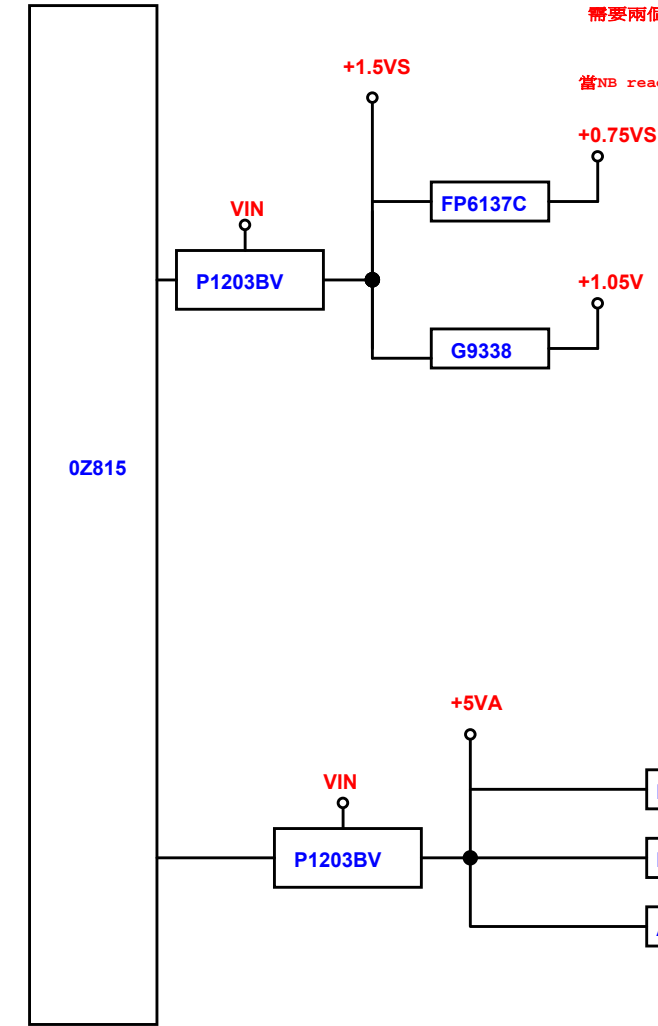
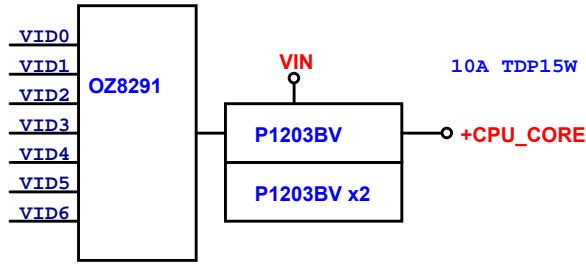
SHUTTLE

SYSTEM BLOCK DIAGRAM

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POWER BLOCK DIAGRAM

System Poewr On Sequence



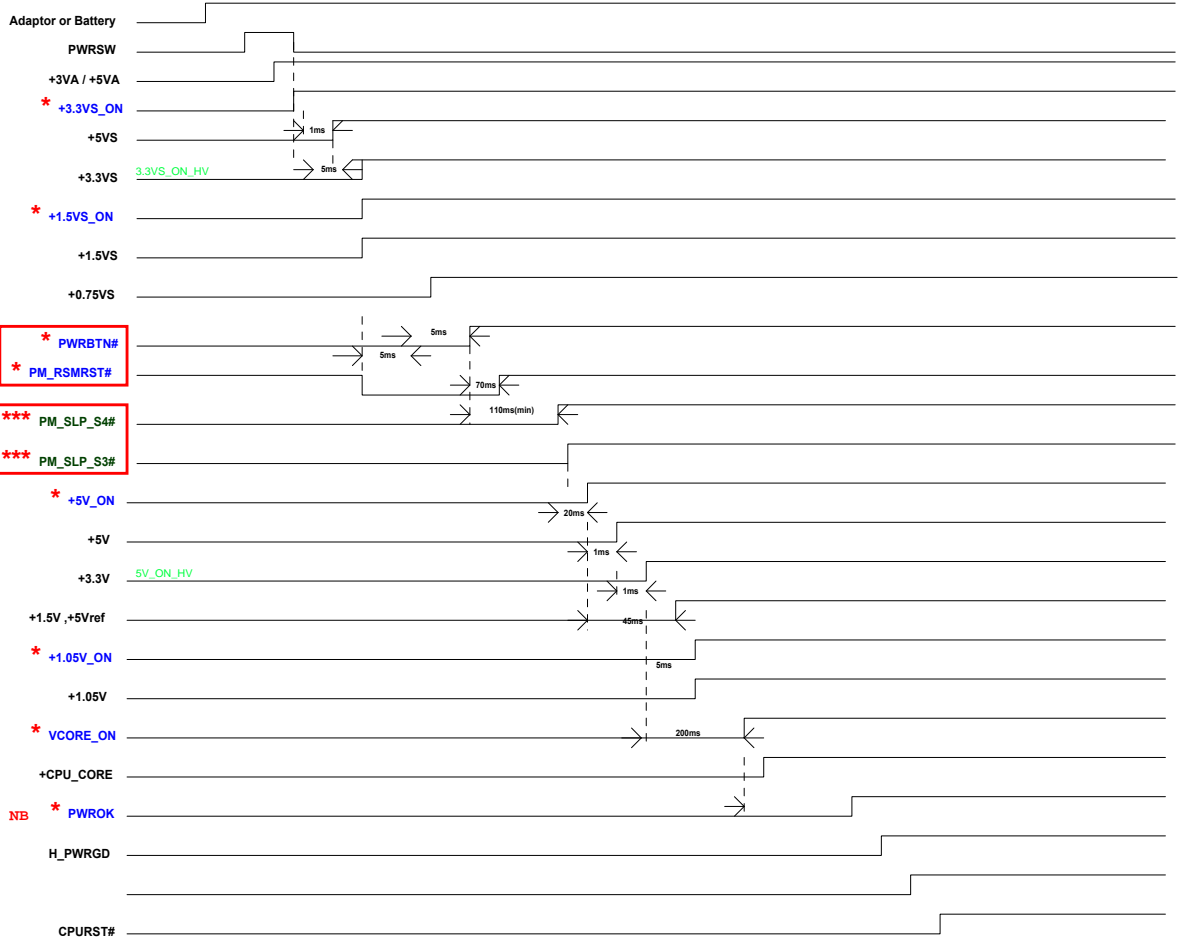
EC發給NB
需要兩個訊號收到後NB才會WORK

當NB ready 時 SUSB SUSC 為HI

EC 發給 NB

- * PWRBTN#
- * PM_RSMRST#
- *** PM_SLP_S4#
- *** PM_SLP_S3#

- * EC Control Pin (O/P)
- ** EC Control Pin (I/P)
- *** NB Control Pin (O/P)



TPT	
GPIO	
GPIO0	AUD_DETECT
GPIO1	4.7K UP TO +5V
GPIO2	PIRQE-
GPIO3	PIRQF-
GPIO4	PIRQG-
GPIO5	PIRQH-
GPIO6	NC
GPIO7	NC
GPIO8	NC
GPIO9	NC
GPIO10	EC_EXTSMI#
GPIO11	ICH_SMBALERT-
GPIO12	10K UP TO +3.3VS
GPIO13	EC_EXTSCI#
GPIO14	NC
GPIO15	10K UP TO +3.3VS
GPIO17	FLASH_STRAP2
GPIO18	
GPIO19	
GPIO20	
GPIO21	
GPIO22	4.7K UP TO +5V
GPIO23	LDRQ1#
GPIO24	GXT_ON#
GPIO25	5K DOWN TO GND
GPIO26	NC
GPIO27	NC
GPIO28	NC
GPIO29	USB_OC#4
GPIO30	USB_OC#6
GPIO31	USB_OC#6
GPIO32	
GPIO33	NC
GPIO34	NC
GPIO35	
GPIO36	4.7K UP TO +3.3V
GPIO37	
GPIO38	NC
GPIO39	NC
GPIO40	
GPIO41	
GPIO42	
GPIO43	
GPIO48	FLASH_STRAP1
GPIO49	CPUPWRGD

ITE8500E		Default
GPIO		Pull/Mode
GPA0	RF_LED_ON#	UP / GPI
GPA1	EC_BSEL0	UP / GPI
GPA2	BTL_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	P_ID0	UP / GPI
GPA5	P_ID1	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	+1.05V_ON	Dn / GPI
GPB3	BAT_SMBCLK	/ GPI
GPB4	BAT_SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Func1
GPB7	PWR_USB#	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMBCLK_EC	/ GPI
GPC2	SMBDAT_EC	/ GPI
GPC3	KEY_OUT16	Dn / GPI
GPC4	SAVE_PWR	Dn / GPI
GPC5	KEY_OUT17	Dn / GPI
GPC6	WLAN_ON	Dn / GPI
GPC7	EC_VID0	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Func1
GPD3	EC_EXTSCI#	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	USB_LED#	UP / GPI
GPD6	+5V_ON	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	Fastcharge_EN	Dn / GPI
GPE2	PWROK	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	+1.VS_ON	Dn / GPI
GPE6	3G_PWR#	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	EC_VID4	UP / GPI
GPF1	3G_ON	UP / GPI
GPF2	EC_VID3	UP / GPI
GPF3	CHG_ON#	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC_VID1	UP / GPI
GPF7	EC_VID2	UP / GPI
GPG0	100K UP TO +3.3VA	Dn/GPO/TM
GPG1	+3.3VS_ON	Dn/GPO/ID7
GPG2	FLFRAME#	
GPG6	WEBCAN_ON	
GPH0	SAFTY_PROTECT	Dn/GPI/ID0
GPH1	+1.8VS_ON	Dn/GPI/ID1
GPH2	SENBAT_V	Dn/GPI/ID2
GPH3	CHG_B_LED	Dn/GPI/ID3
GPH4	CHG_R_LED	Dn/GPI/ID4
GPH5	BATTOFF	Dn/GPI/ID5
GPH6	PWR_LED	Dn/GPI/ID6

ITE8500E		Default
GPIO		Pull/Mode
GPI0	NC	/GPI
GPI1	LCDSW0	/GPI
GPI2	LCDSW1	/GPI
GPI3	NC	/GPI
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTER_I	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_EN	/GPI/DAC
GPJ1	EC_PROCHOT#	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	CRT_DETECT	/GPI/DAC

PINEVIEW-D					
	CPU	CORE (V)	ICC (A)	W	TEMP (°C)
IMVP-6+	1.2	3	3.3	90	

TPT					
	CPU	CORE (V)	ICC (A)	W	TEMP (°C)
IMVP-6+	1.2	3	3.3	90	

ITE8500E			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	100	330	70

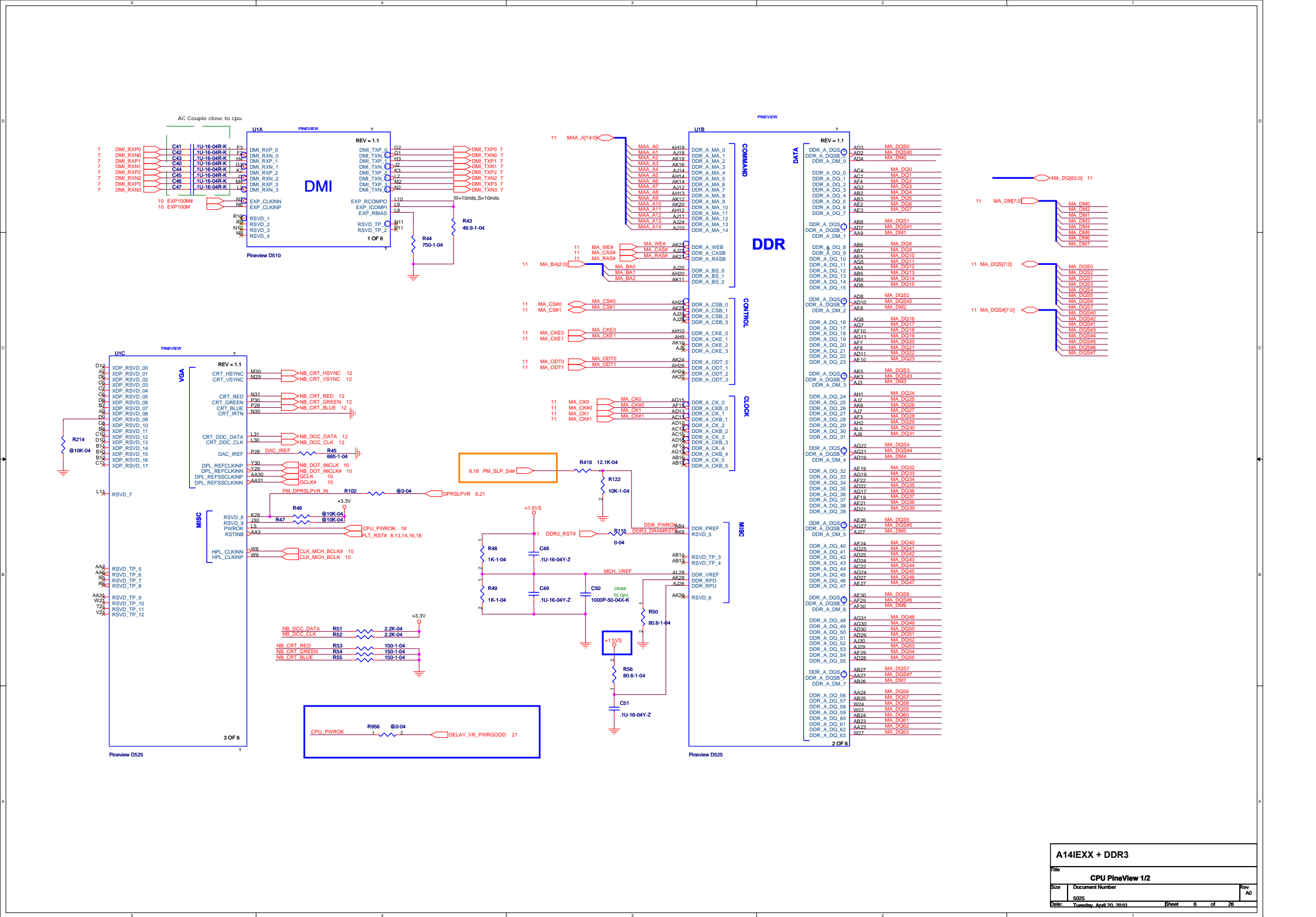
CLOCK GENERATOR			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	250	825	70

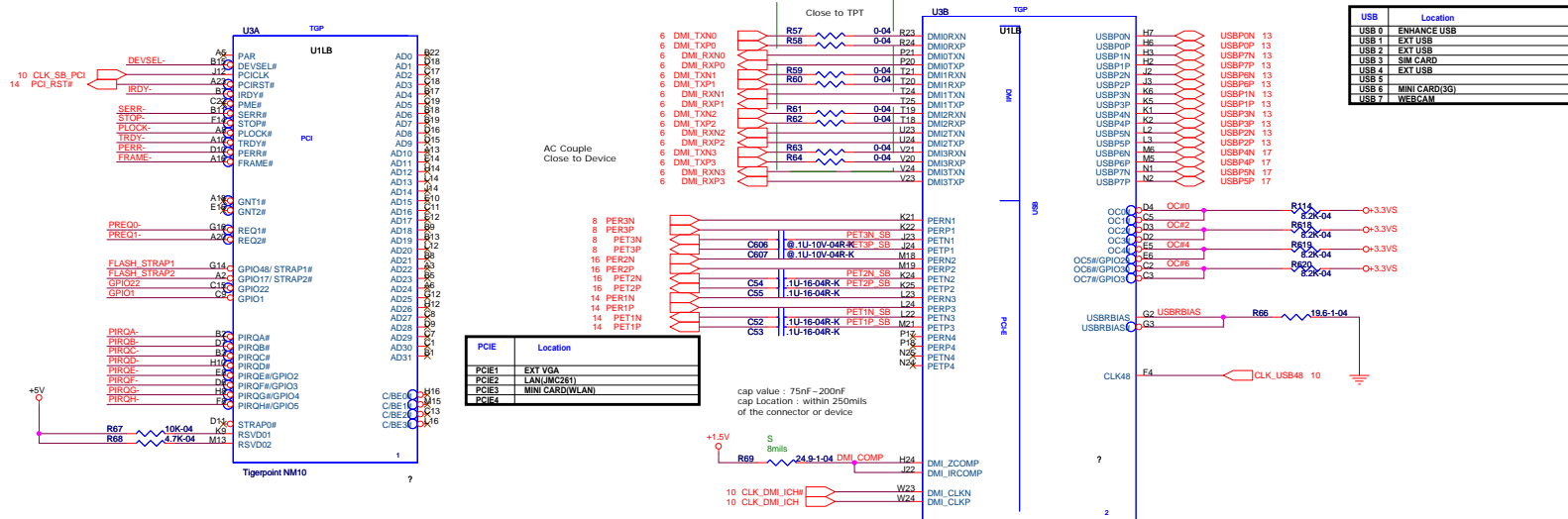
EMC1402			
VCC	ICC	mW	TEMP (°C)
+3.3V	170uA	0.56	150

CODEC			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	250	825	70

JMC261			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	250	825	70

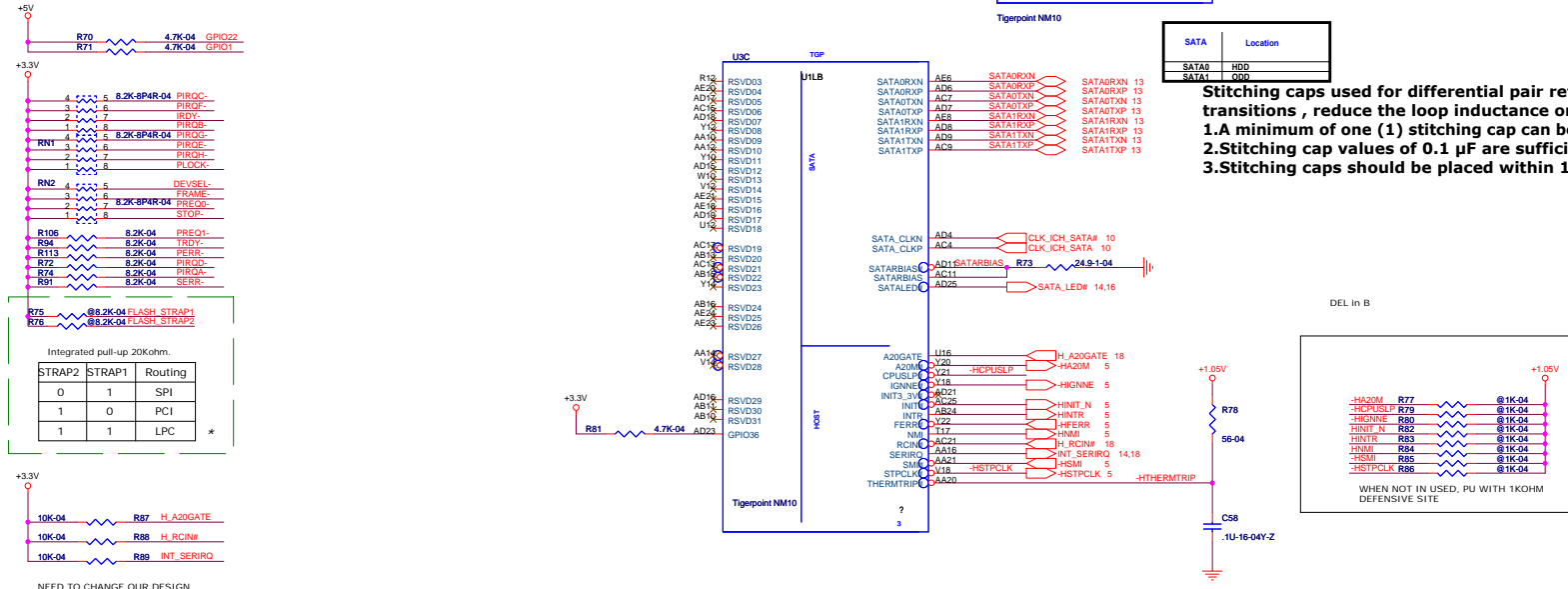
SHUTTLE			
GPIO & Power Consumption			
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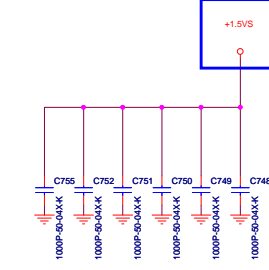
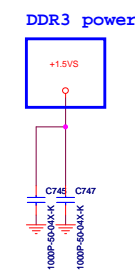
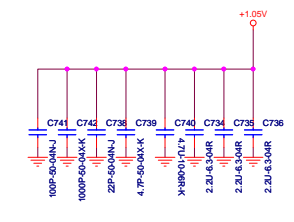
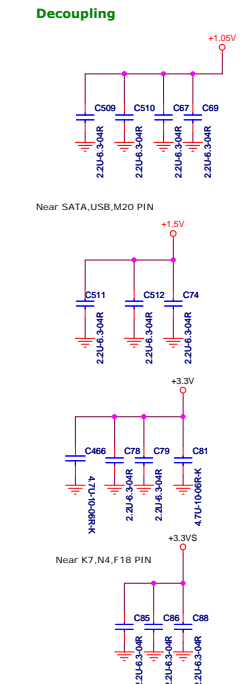
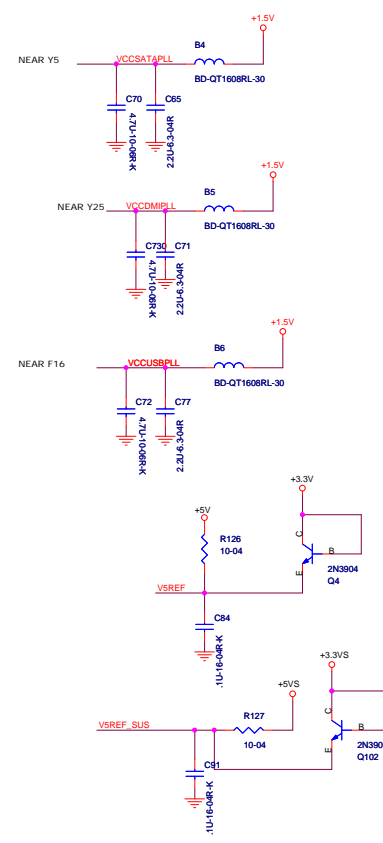
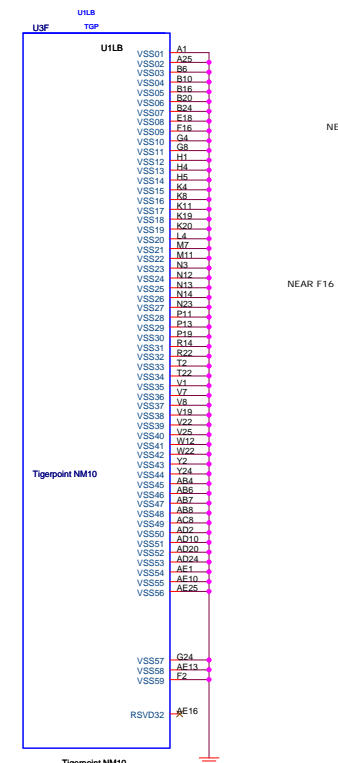
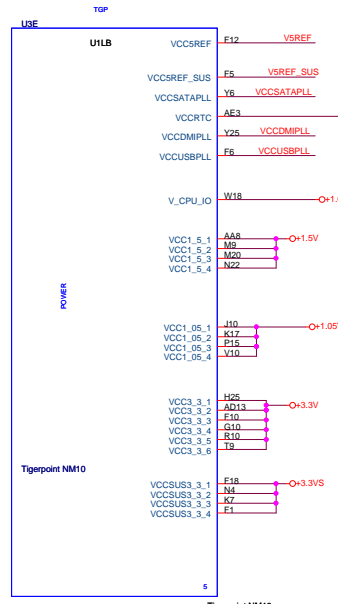




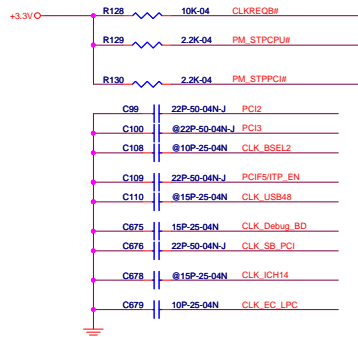
Stitching caps used for differential pair reference plane transitions, reduce the loop inductance on the currents return path

1. A minimum of one (1) stitching cap can be shared by up to four different pairs.
2. Stitching cap values of 0.1 μ F are sufficient.
3. Stitching caps should be placed within 100 mils





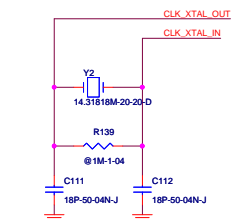
A14IEXX + DDR3			
Title			
TPT Power			
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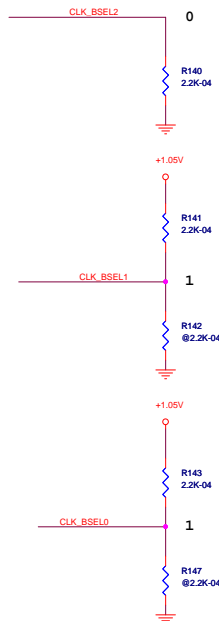
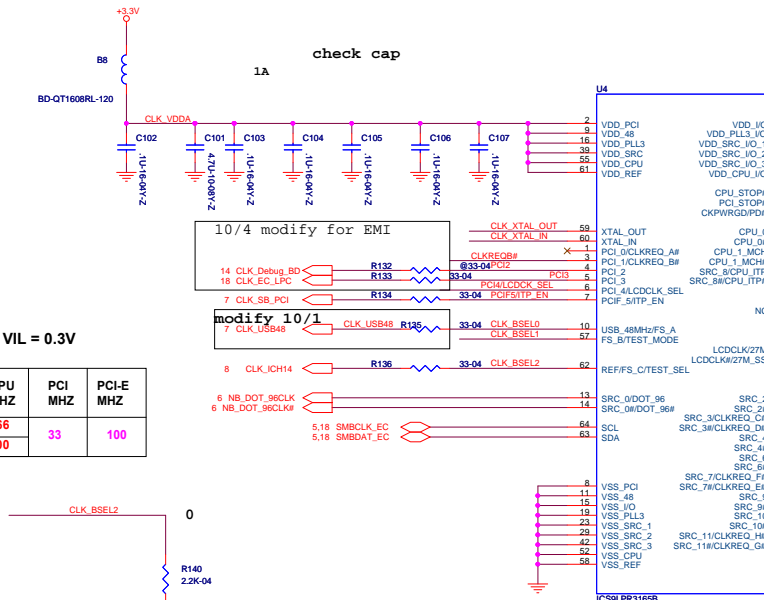
Reserved FOR EMI

Bsel [0..2] VIH = 0.7V VIL = 0.3V

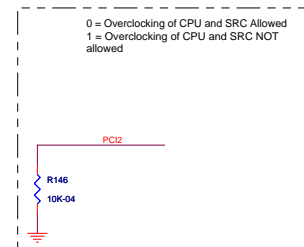
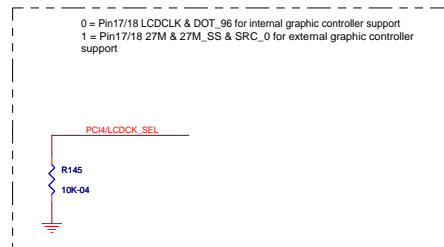
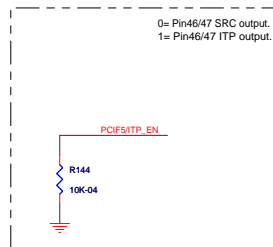
FSB	BSEL	BSEL2	BSEL1	BSEL0	CPU	PCI	PCI-E
		FSLC	FSLB	FSLA	MHZ	MHZ	MHZ
FSB533	0	1	1	166	33	100	
FSB667	0	1	0	200			



$C_e = 2 * C_L - (C_s + C_i)$
 C_L = Crystal Load Cap = 20p
 C_i = IC internal Cap = 5p
 C_s = 2p
 C_e = Crystal external Cap = 33p



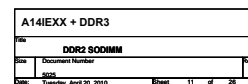
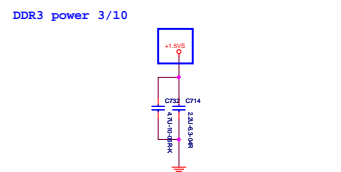
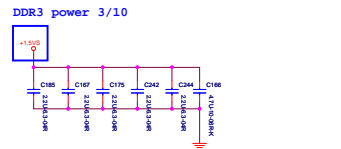
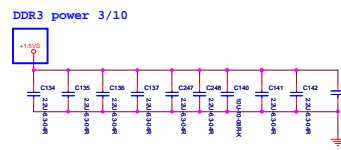
@Check EC Code programing before vcore ready.



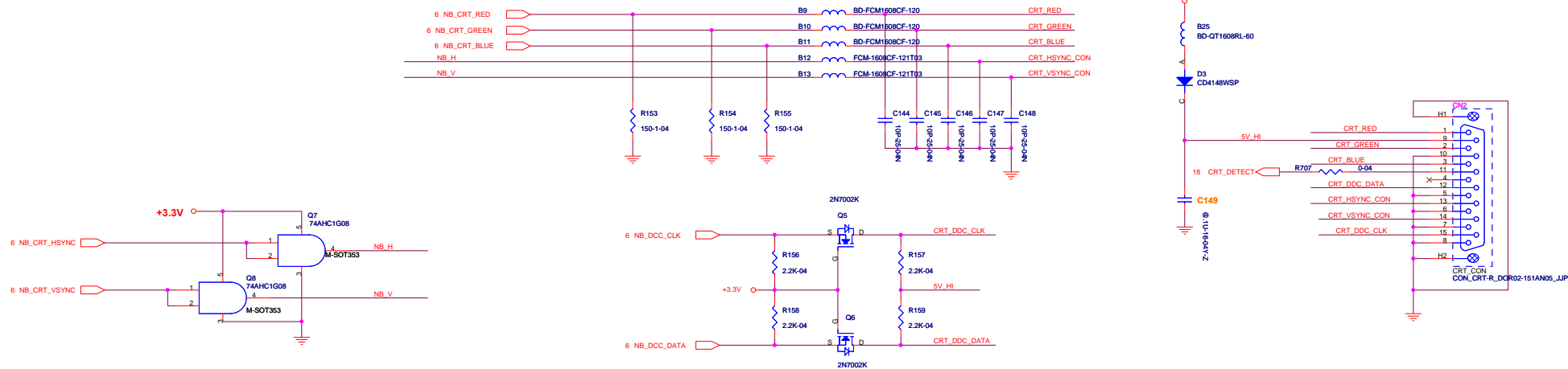
A14IEXX + DDR3

CLOCK GEN (ICS9LPR365)

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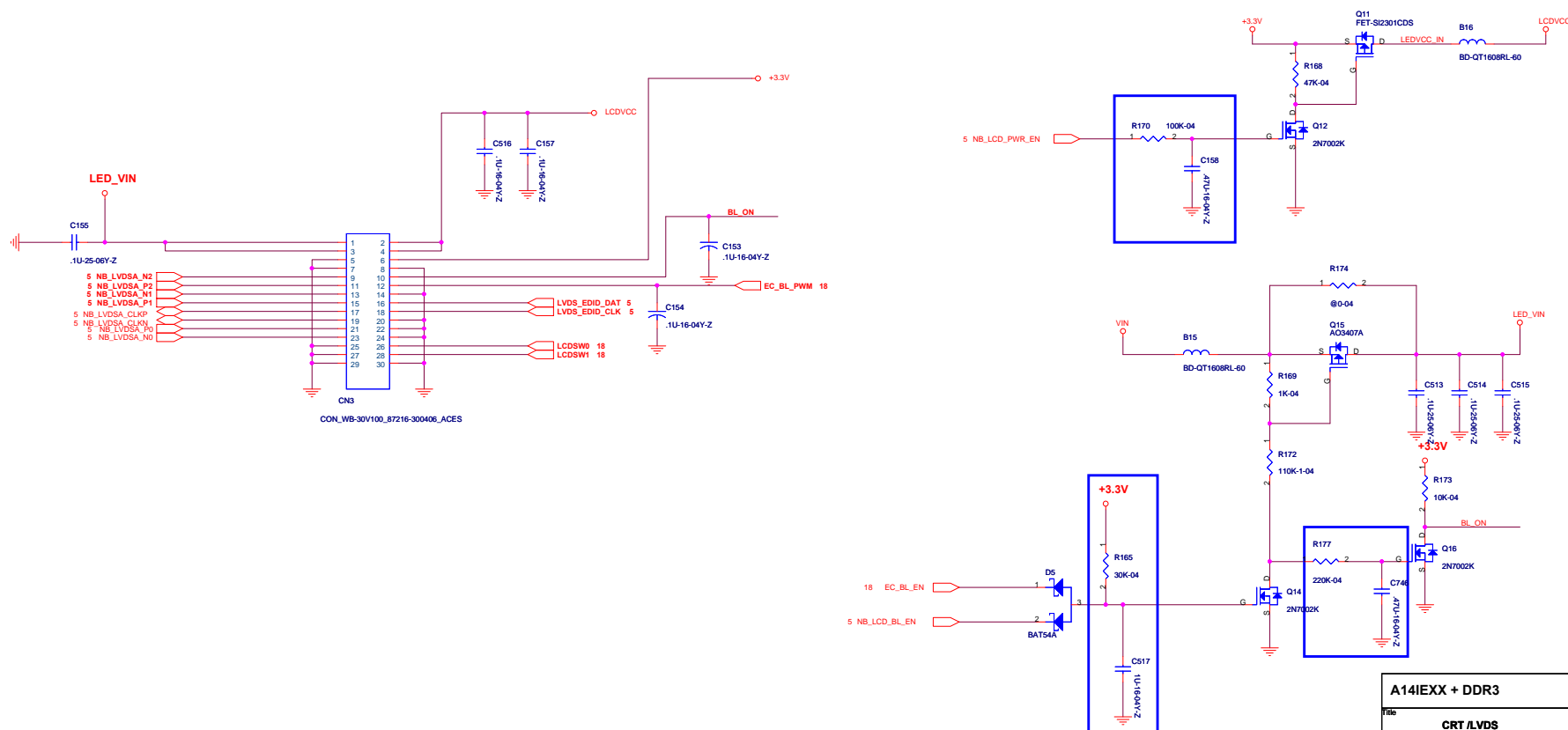


VGA Conn.



LVDS

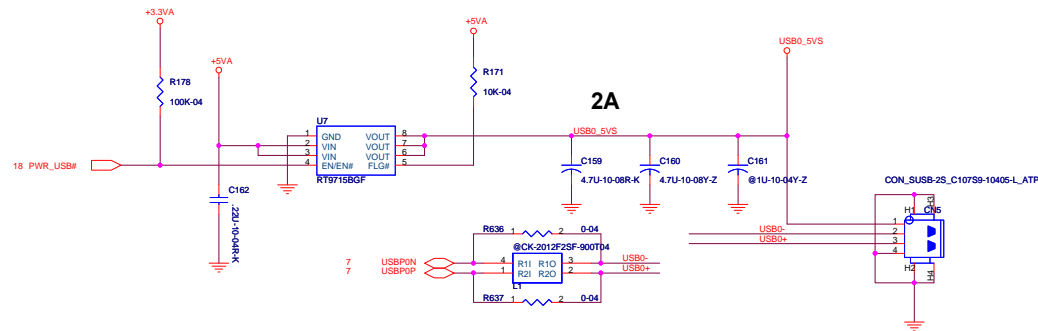
LED option



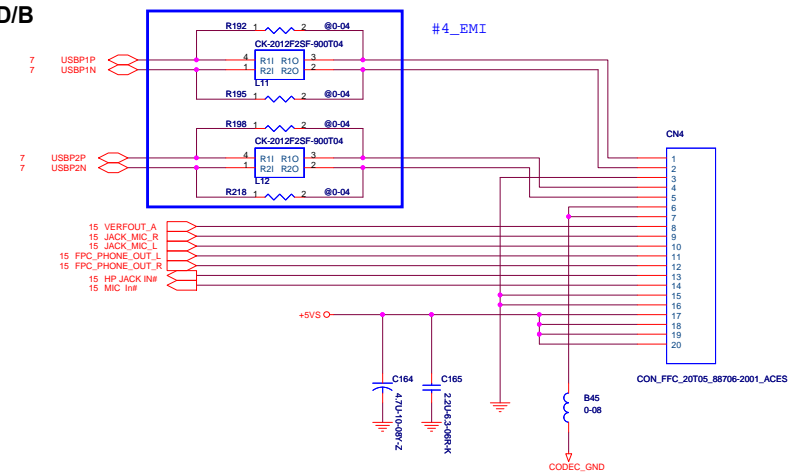
A14IEXX + DDR3

CRT /LVDS		
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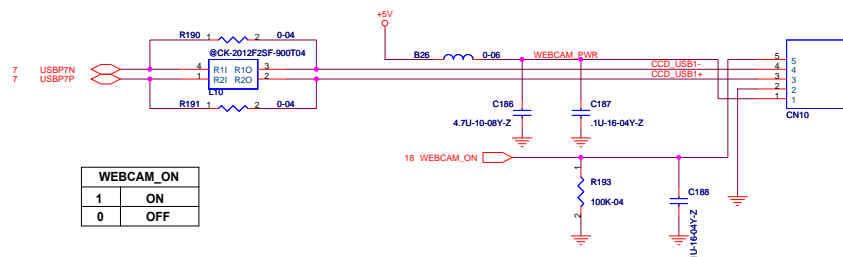
ENHANCE USB



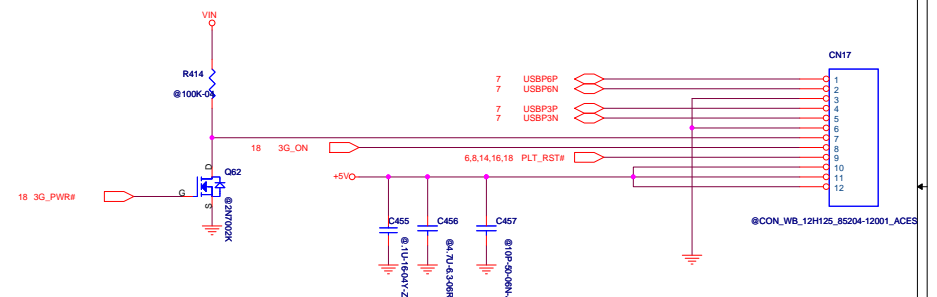
USB D/B



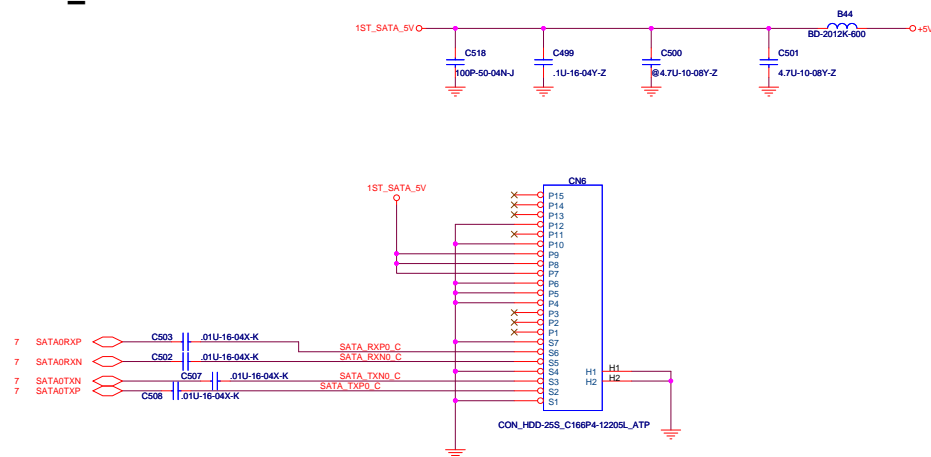
WEBCAM



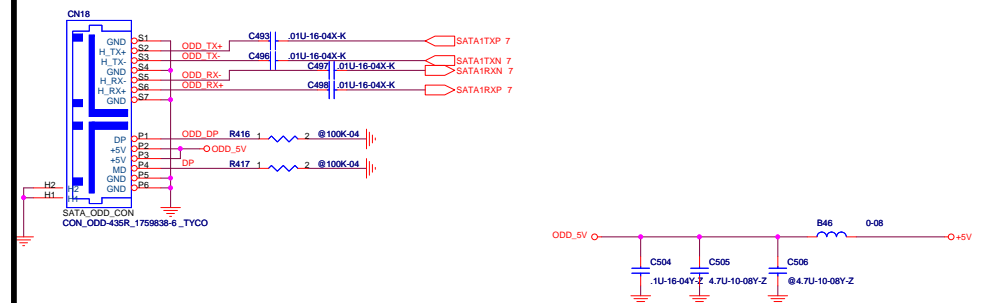
3G_D/B



SATA_HDD



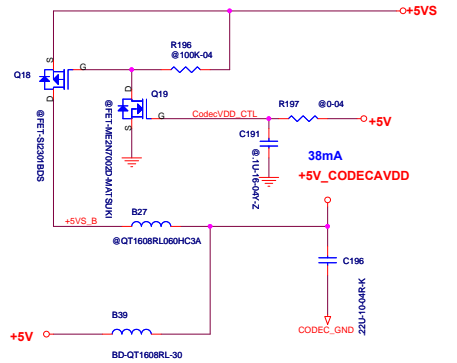
SATA_ODD



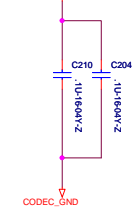
A14IEXX + DDR3

13 USB / WEBCAM / SATA / BT			
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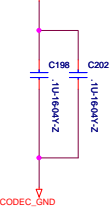
AMP VDD



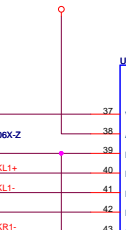
+5V_CODECAVDD



+5V_AMP



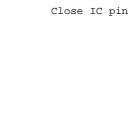
+5V_CODECAVDD



+5V_AMP

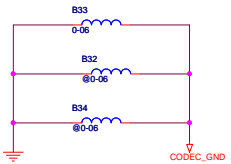


+3.3V

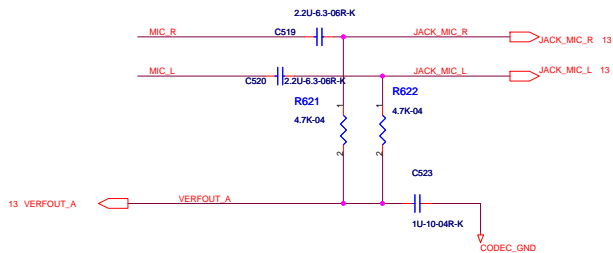
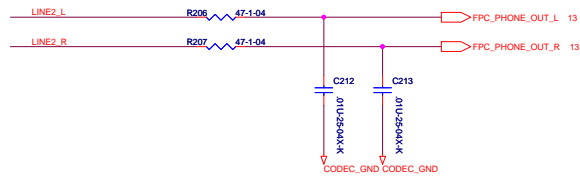


USE 80 MILLS WIDE TRACE
LOCATE UNDER CODEC.

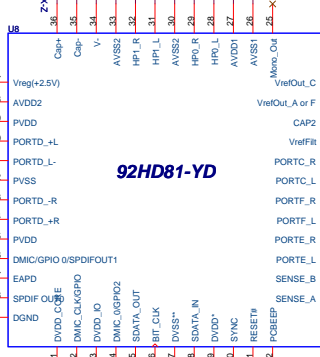
BRIDGING AGND AND DGND PLANES



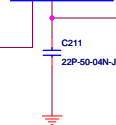
HEADPHONE



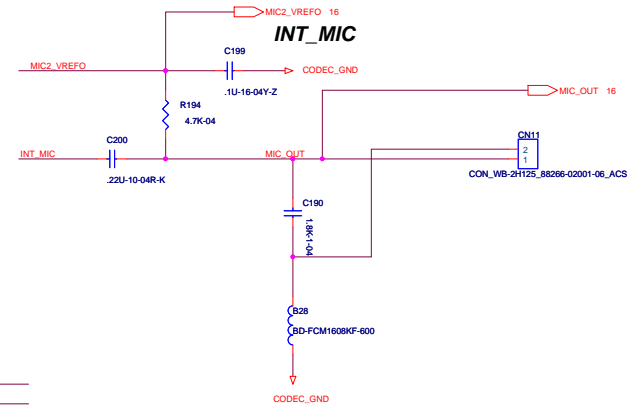
92HD81-YD



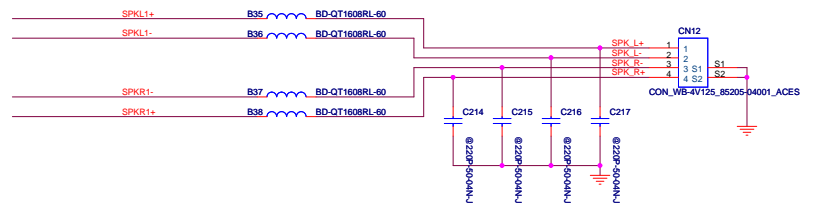
#1_EMI



INT_MIC



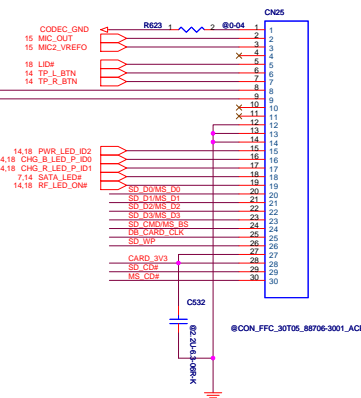
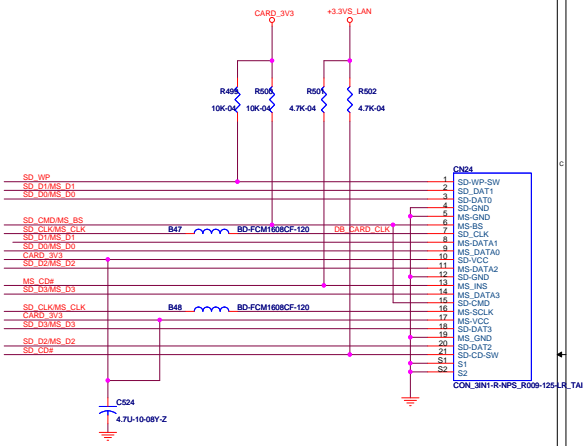
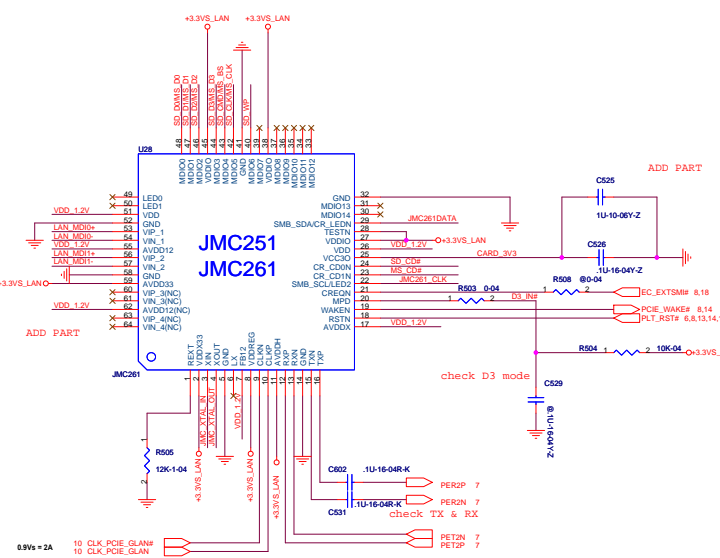
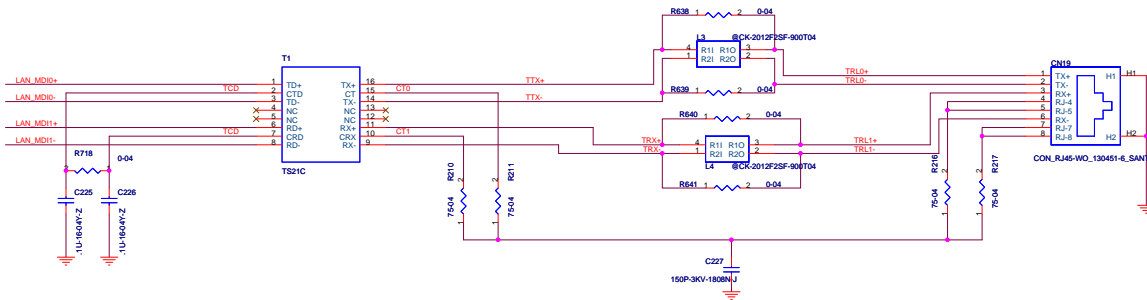
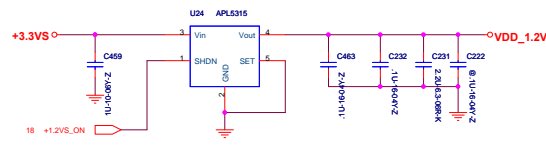
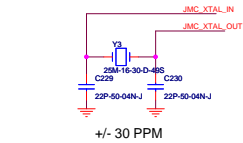
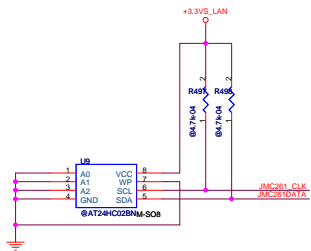
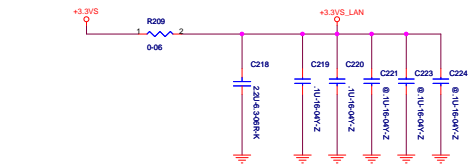
SPEAKER



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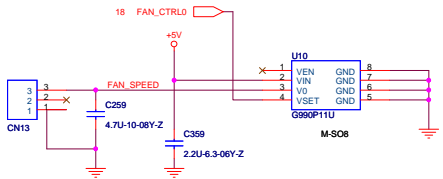


SHUTTLE		
File	15 CODEC & AMP/INT_MIC/SPK	
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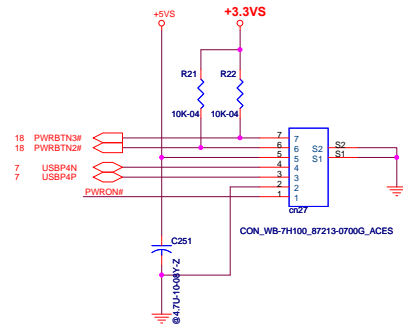
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FAN



CON_WB-3H125_85204-03001_ACES

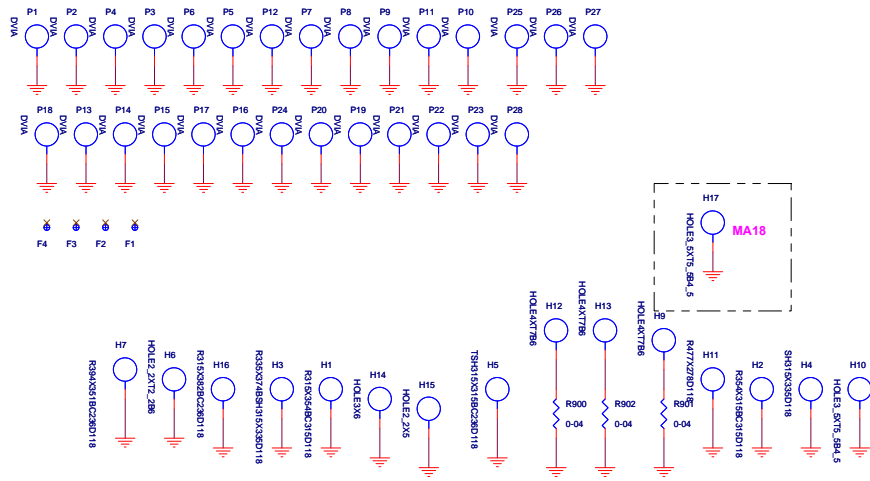
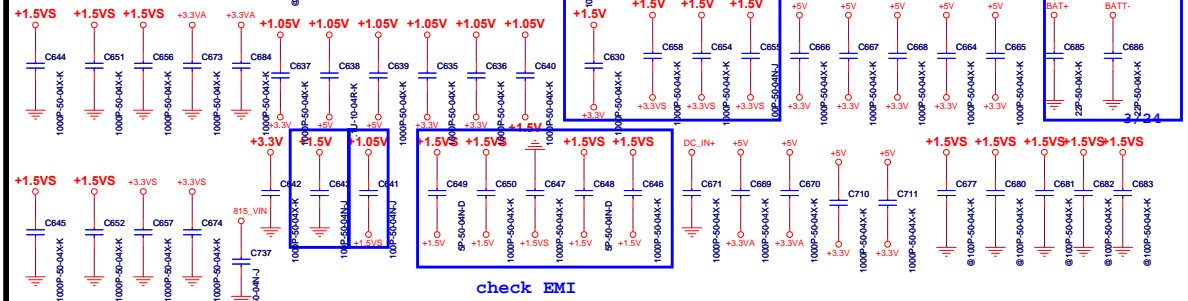
USB SWITCH



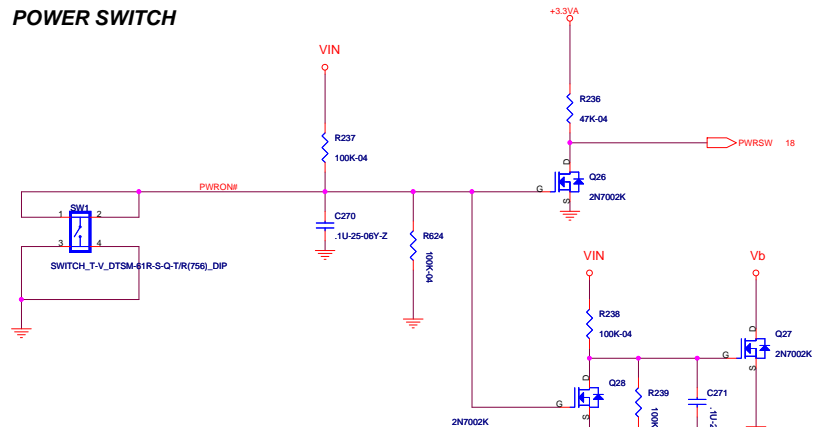
CON_WB-7H100_87213-0700G_ACES

AC-CAP

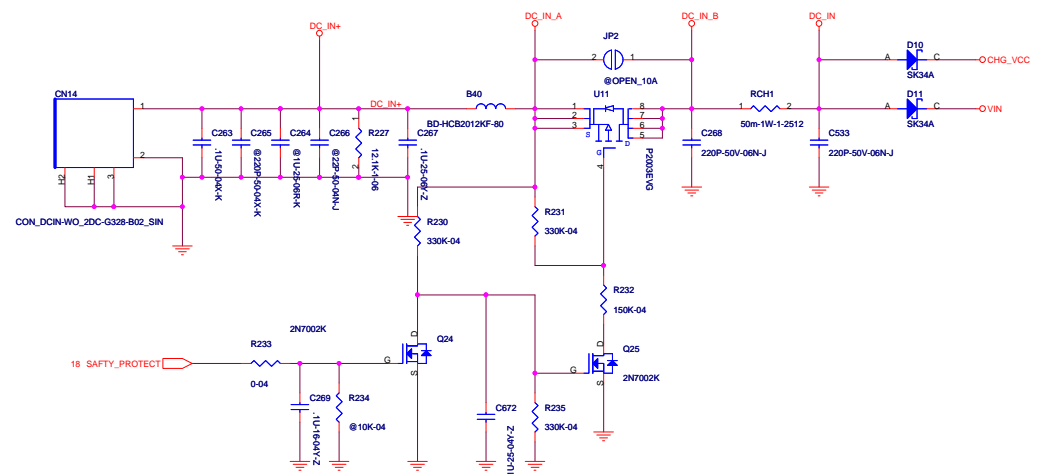
CHECK EMI #5_EMI



POWER SWITCH

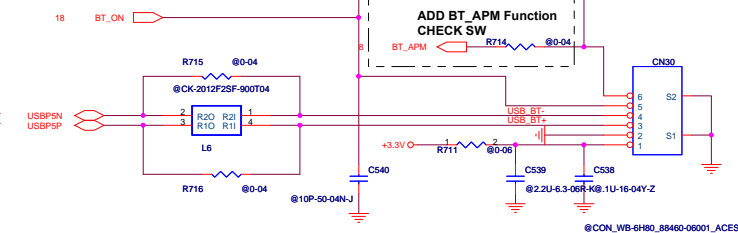


DC-IN



BT CONN

MA13

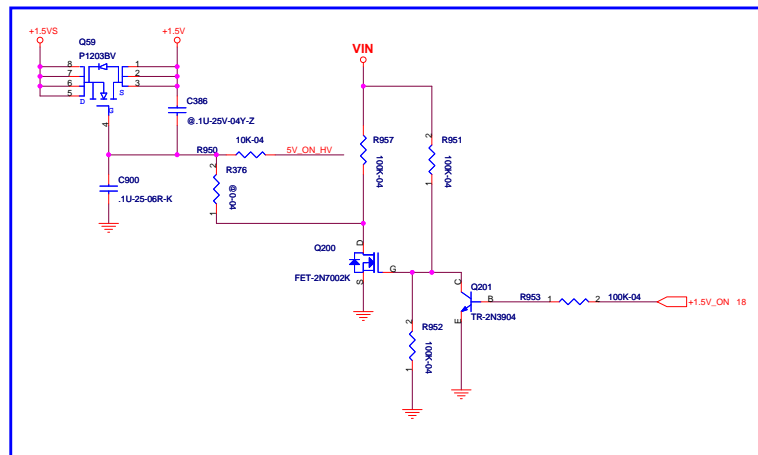
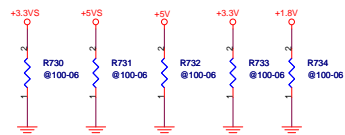
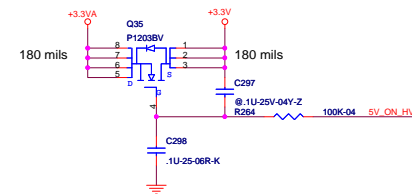
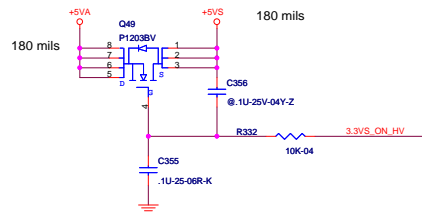
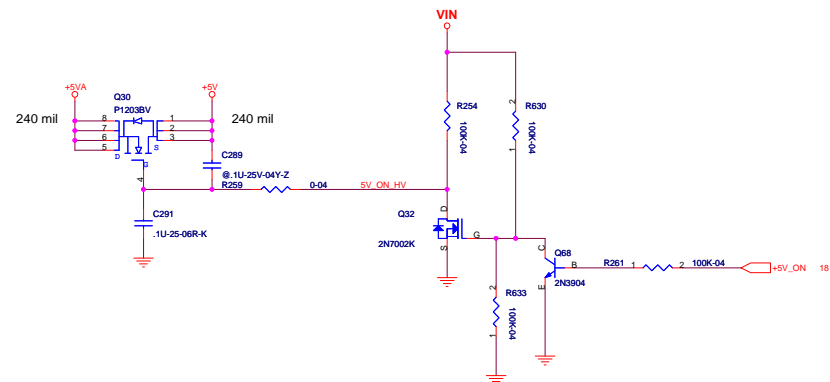
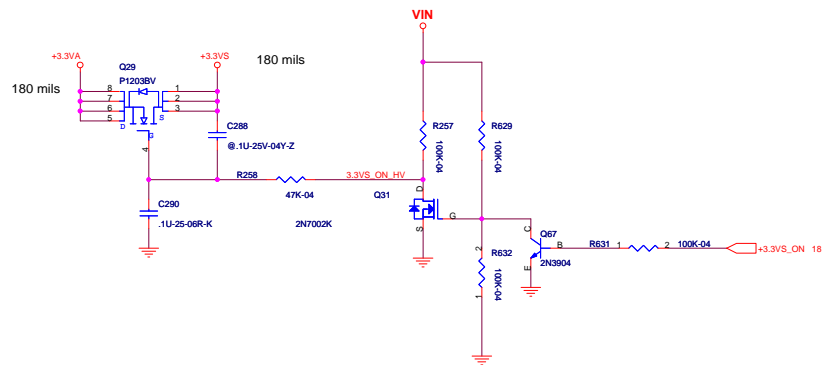


modify 9/28

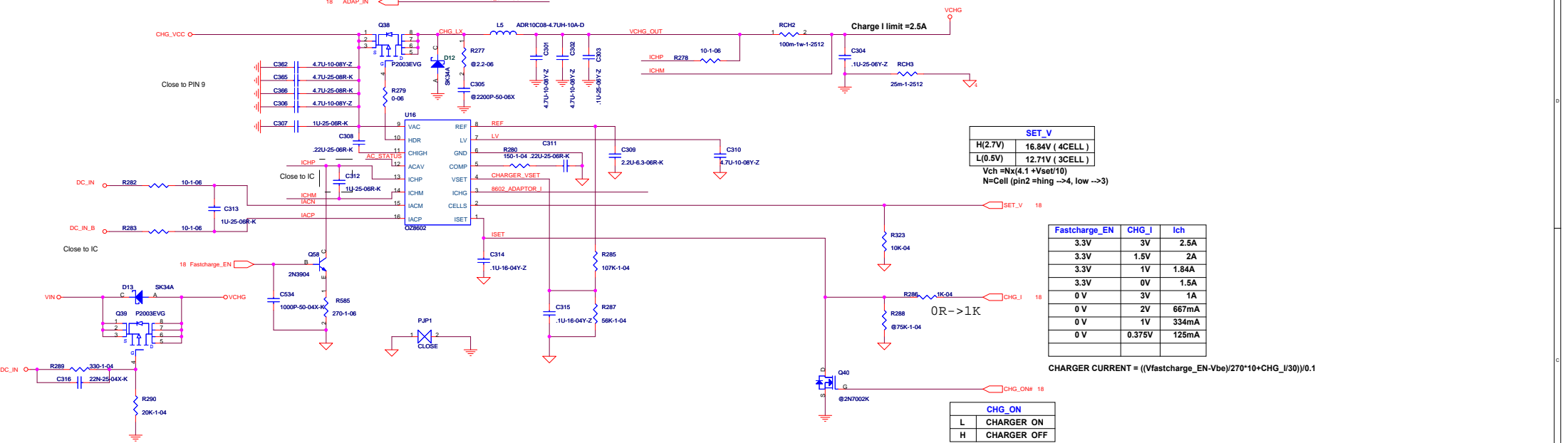
CHECK BT TYPE AND Life power function

File			PWR SW/FAN/HSCRP CAP/DC IN
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5025			
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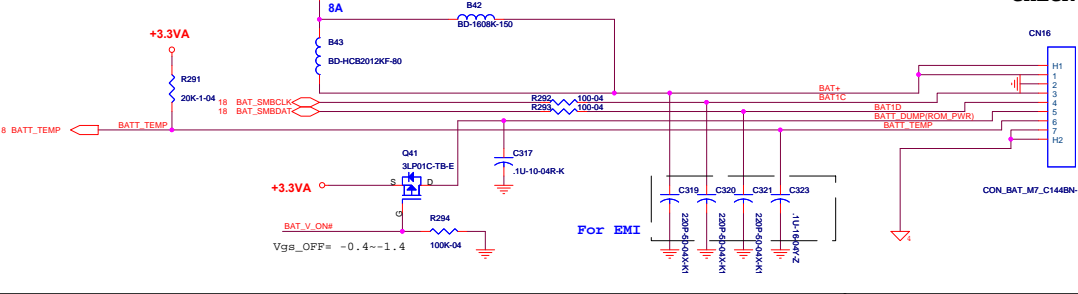
VCC SW



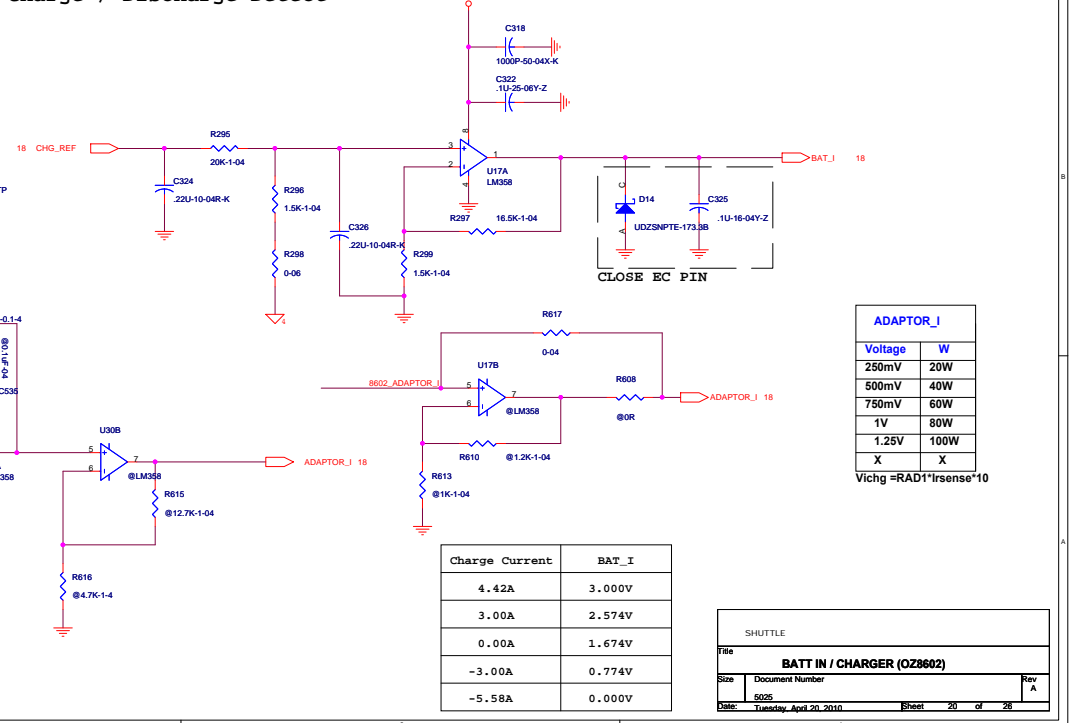
CHARGER



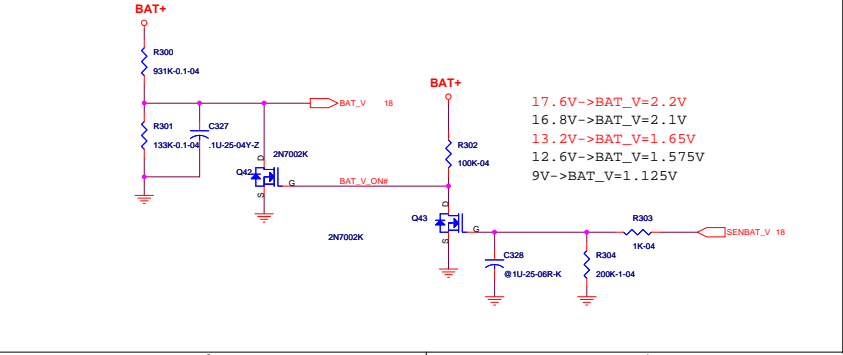
BATTERY CON

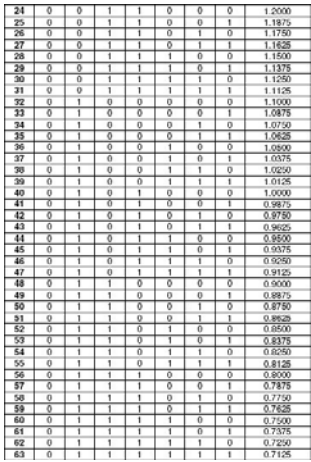


Charge / Discharge Detect



Battery Voltage Detect





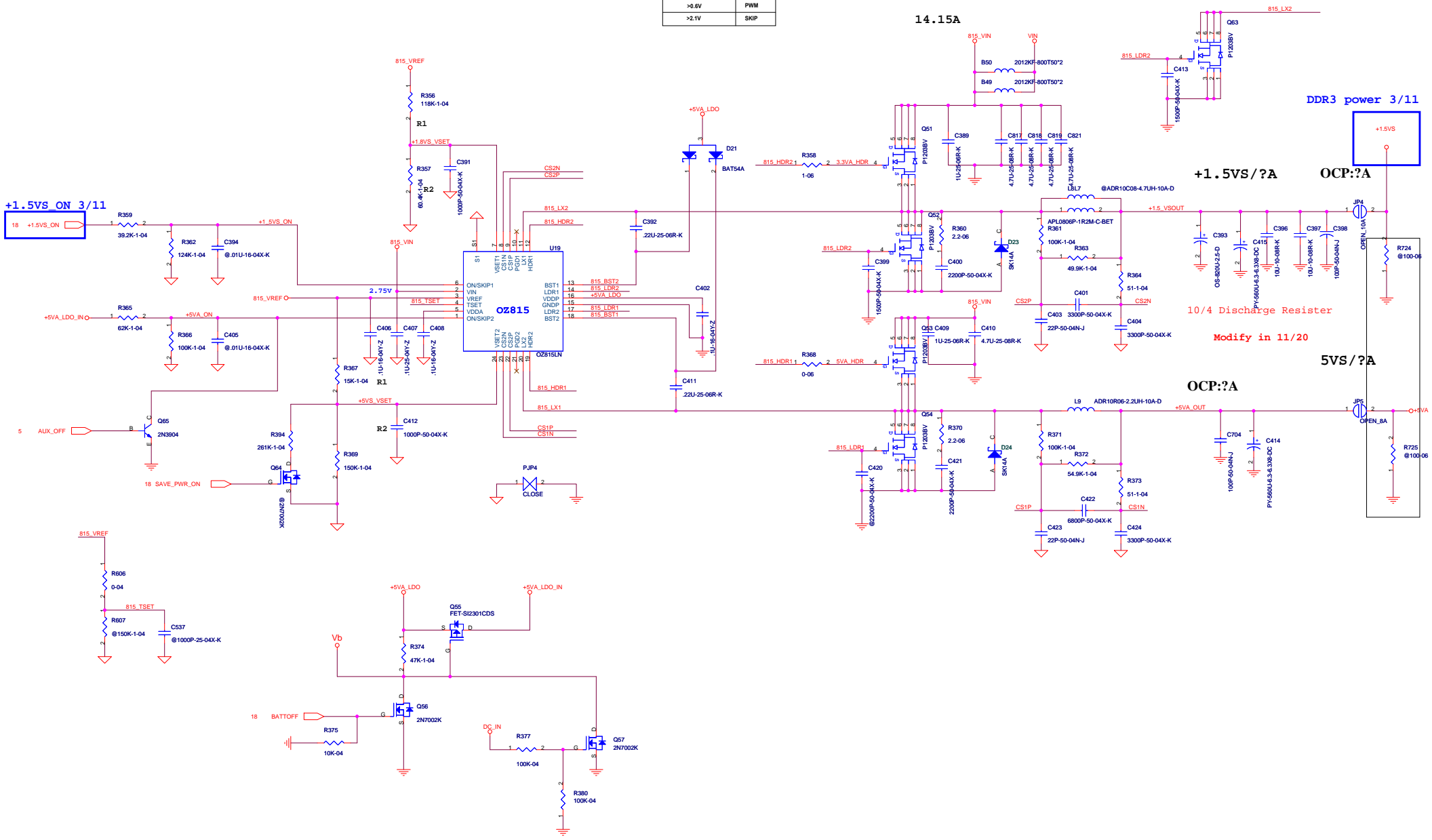
SHUTTLE			
File CPU CORE (OZ8291)			
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+1.8V/+5V_Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

$$\text{Output Voltage} = \left[\text{Vref} \times \frac{R2}{R1+R2} \right] \times 2$$

14.15A

+1.5VS ON 3/11



RB change list:

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SHUTTLE		
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RC change list:

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SHUTTLE			
File			
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T10IL1 Power on Sequence Diagram

